HDRR-3.6G-12B

PRECISION RECEIVERS

Precision Receivers Incorporated Introduces 1st HDRR Receiver

The HDRR-3.6G-12B is a single-channel signal collection and recording system incorporating PRI proprietary technology to reduce spurious responses in the analog to digital converter. The system collects and records signals across a large (>1GHz) BW. HDRR technology is described as the industry's most effective way to improve the performance of direct-sampled receivers employed in electronic warfare, radar, signals and communications intelligence, spectrum monitoring, and wireless communications systems. HDRR technology provides an order-of-magnitude improvement in reducing unwanted spurious signals to levels previously unachievable using other methods and increases spurious-free dynamic range (SFDR) by up to 16 dB.

The formfactor is designed for low cost and is ideal for low-profile applications. Figure 1 describes the block diagram of the system.

HDRR™ High Dynamic Range Receiver Key Features

- ♦1.75 GHz IBW Single CH
- ♦11.4 Bits ENOB
- ♦80 dB SFDR Typical
- ♦2.5 Gsps Single CH
- ♦Digitally Reject Nyquist Zones
- ♦Commercial Computer Form Factor
- ♦300 Sec DRFM continuous recording @ Full Bandwidth in demonstration configuration unit

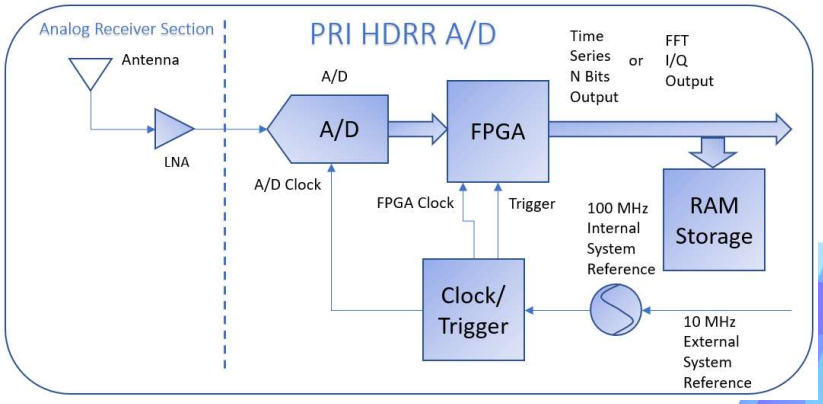

Figure 1: Block diagram of PRI System

Precision Receivers Incorporated (PRI) New technology

PRI has introduced proprietary technology to reduce spurious responses in analog to digital converter systems. All ADCs have quantization and timing errors creating spurs in the outputs of ADCs. These spurs degrade the sensitivity of Cellular, SIGINT, COMINT, ELINT and EW systems. Many schemes have been implemented to mitigate these problems such as clock dithering, but the schemes have tradeoffs and consequences including a reduction in the dynamic range of a system. PRI's technology reduces the magnitude of all the spurs across the IF bandwidth and over the entire RF input bandwidth, nearly the entire Fs/2 as well as all the Nyquist zones. Figure 2 (next page) shows the ENOB performance of PRI's new technology, current ADC chips and a competitor's digitizer board. Figure 3 shows the SNR performance of PRI's new technology. Existing competitive 2.5 GSPS systems struggles to achieve 10 effective bits or ENOB. PRIs technology achieves almost 11.5 bits of ENOB. Increased performance will serve to enhance future systems and PRI's technology allows for an easy upgrade to existing platforms. Other BW's are available as well as other clock rates and more ruggedized formfactors are being developed.

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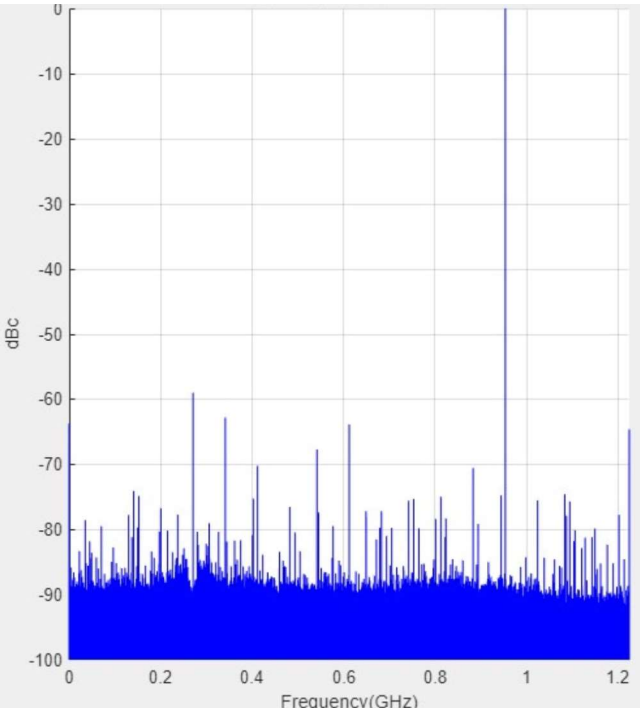
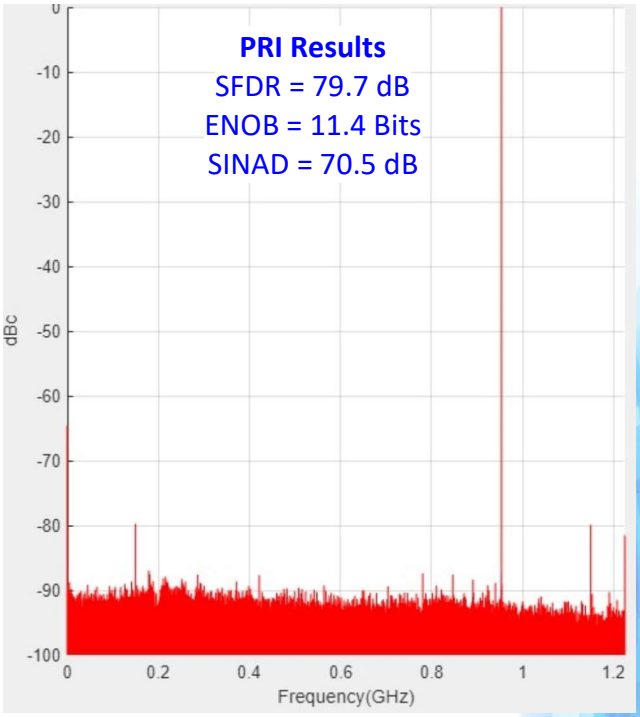
Figure 2 Nyquist Zone 1 954 MHz CW Sample Rate 2300 MHz Lab Test Data Results



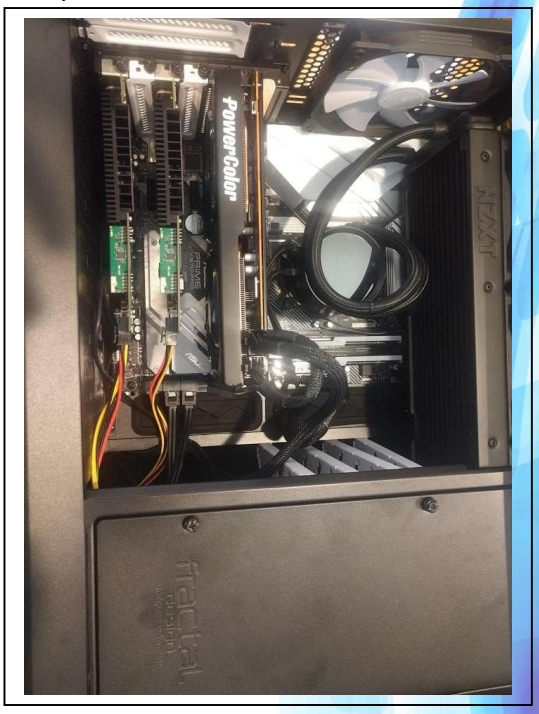
Zone 1
954 MHz
Improvements
SFDR = 20.6 dB
ENOB = 2.0 Bits
SINAD = 12.0 dB

Typical Results
SFDR = 59.1 dB
ENOB = 9.4 Bits
SINAD = 58.5 dB



Precision Receiver's High Dynamic Range Receiver (HDRR) technology uses a unique technology to avoid spur generation. There is no calibration or *a priori* information necessary over temperature or time to mitigate the spurs across the entire bandwidth although there may be calibration for your application. The technology also allows the ability to null, cancel or tune out other undesired Nyquist zones, cancelling adjacent Nyquist zone ghosting by 50 - 80 dB. This additional benefit to the system architecture will relax anti-alias filter specifications.

Form Factor: Desktop PC
Instantaneous Bandwidth: 1.75 GHz, 1 GHz Realtime
Maximum Clock Rate: 3.6 Gsps, 2.0 Gsps Realtime
ADC bit depth (no decimation): 12 bits
ADC device Memory: DDR4 SDRAM 5 GB 1200 MHz (2400 MHz DDR)
Two Xilinx Kintex UltraScale FPGA units per system
Storage: 2 TB of High-Performance storage
Power
Voltage: 120 V
Watts: 750 W
Cycles: 50-60 Hz



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